REMARKS

Claims 63-70 and 72-92 are pending in this application, with claims 63, 70, 73, 74, and 77-80 being independent. Claims 63-69, 72-76, 78-80, 82, and 84-86 have been withdrawn from consideration. Claims 70 and 77 have been amended. Claims 1-62 and 71 have been canceled, and claims 87-92 have been newly added. Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

Claim Rejection – 35 U.S.C. § 103

Claims 70, 77, and 83 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication Number 2003/0127667 ("Inoue") in view of U.S. Patent Application Publication Number 2003/0030089 ("Sumino"). Claim 81 was rejected under § 103(a) as being unpatentable over Inoue in view of Sumino and further in view of U.S. Patent Number 6,433,400 ("Gardner"). Applicants respectfully traverse these rejections for at least the following reasons.

As amended, claim 70 recites a method for manufacturing a solid-state imaging device in which an imaging region in which a plurality of unit pixels are arranged is provided on a semiconductor substrate. Each of the unit pixel includes a plurality of element formation regions and an element isolation formation region located between the plurality of element formation regions. The method includes a step (a) of forming, on the semiconductor substrate, a protection film including an opening portion that exposes the element isolation formation region and a region of an upper face located beside the element isolation formation region of the semiconductor substrate. The method also includes a step (b) of forming a sidewall on a side

face of the opening in the protection film; a step (c) of forming a trench in the element isolation formation region in the semiconductor substrate by etching using the protection film and the sidewall as a mask; and a step (d) of oxidizing a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after step (c) to form an inner wall thermal oxide film.

Additionally, the method includes a step (e) of forming an element isolation region by burying the trench with a burying film after the step (d); and a step (f) of forming a photoelectric conversion section and an active region in the element formation regions after the step (e). In step (c) the width of the trench is made smaller by the thickness of the sidewall than the width of the opening in the protection film, and in step (f), the photoelectric conversion section and the active region are arranged apart from the element isolation region by the thickness of the sidewall. In step (d), the inner wall thermal oxide film, due to the sidewall formed on the side face of the opening in the protection film, is formed to an edge of the semiconductor substrate which is located at an upper edge portion of the trench.

To provide context, FIG. 1C of the instant application illustrates a trench (6) formed in the element isolation formation region in the semiconductor substrate (1) by performing etching by using the protection film (2) and the sidewall (5) as a mask. Then, as shown in FIG. 1D, a portion located at the side face of the trench (6) in the semiconductor substrate (1) is oxidized by using the sidewall (5) formed only on a side face of the opening (4) in the protection film (2) as a mask to form an inner wall thermal oxide film (7). As a result, the inner wall thermal oxide film (7) is formed to an edge of the semiconductor substrate (1) which is located at an upper edge portion of the trench (6). Thereafter, as shown in FIG. 1F, a photoelectric conversion section (9) and an active region (10) are formed on the semiconductor substrate (1).

In this manner, the inner wall thermal oxide film (7) can be formed to an edge of the semiconductor substrate (1), which is located at an upper edge portion of the trench (6) since the sidewall (5) is formed on the side face of the opening in the protection film (2) and not on the side face of the semiconductor substrate (1). As a result, the formation of the inner wall thermal oxide film (7) allows an edge of the semiconductor substrate (1), which is exposed at the upper edge portion of the trench (6) to be rounded, thereby preventing field concentration at the edge of the semiconductor substrate (1) in operation of the device. *See e.g.*, Published Application at page 9, paragraph [171].

Applicants respectfully request reconsideration and withdrawal of the rejection of claim 70 because Sumino and Inoue, either alone or in combination, fail to describe or suggest a method that includes, among other steps, a step (c) of forming a trench in an element isolation formation region in a semiconductor substrate by etching using a protection film and a sidewall as a mask, and a step (d) of oxidizing a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after step (c) to form an inner wall thermal oxide film, wherein in step (d), the inner wall thermal oxide film, due to the sidewall formed on the side face of the opening in the protection film, is formed to ***an edge*** of the semiconductor substrate which is ***located at an upper edge portion*** *of the trench*, as recited in claim 70.

The Office Action concedes that Inoue fails to describe or suggest the above-recited features of claim 70. *See e.g.*, Office Action at page 2, lines 24-26 (stating Inoue does not disclose the specific steps (a)-(e) in forming trench isolation regions). Therefore, the Office Action relies on Sumino to remedy the shortcomings of Inoue. In particular, the Office Action relies on FIG. 1A-1D of Sumino to describe or suggest the above-recited features of claim 70.

Sumino, in the relied upon portions, describes a method for manufacturing a semiconductor device. The method includes the steps of forming an opening in a nitride film (30) on a semiconductor substrate (10) and thereafter etching the semiconductor substrate (10) using the nitride film (30) as a mask to form a first recess serving as an upper trench (40a) on the semiconductor substrate (10). *See e.g.*, Sumino at page 3, paragraph [42] and FIG. 1A. Referring to FIGS. 1C and 1D of Sumino, the method also includes steps of forming a sidewall (50b) on a side face of the opening in the nitride film (30) and of the upper trench (40a) and etching the semiconductor substrate (10) using the sidewall (50b) as a mask to form a second recess serving as a lower trench (40b). *See e.g.*, Sumino at page 3, paragraph [43].

Additionally and referring to FIG. 1E of Sumino, the method includes the steps of oxidizing a side face of the lower trench (40b) using the sidewall (50b) as a mask to form an internal wall oxide film (50c) on the side face of the lower trench (40b). *See e.g.*, Sumino at page 3, paragraphs [43, 44]. As such, in the relied upon portions, the internal wall oxide film (50c) only forms on the side face of the lower trench (40b) and does not form on the side face of the upper trench (40a). That is, because the sidewall (50b) covers both the side face of the opening and the side face of the substrate (e.g., upper trench (40a)), the side face of the upper trench (40a) is not oxidized. Therefore, the inner wall thermal oxide film (50c) is *not* formed to *an edge* of the substrate (10) *located at an upper edge portion of the trench*.

In contrast, in claim 70, the inner wall thermal oxide film (7) *is* formed to *an edge* of the semiconductor substrate, which is *located at an upper edge portion of the trench* since the sidewall is formed only on the side face of the opening in the protection film and not on the side face of the substrate. Accordingly, in the relied upon portions, Sumino fails to describe or suggest a method that includes, among other steps, a step (c) of forming a trench in an element

isolation formation region in a semiconductor substrate by etching using a protection film and a sidewall as a mask, and a step (d) of oxidizing a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after the step (c) to form an inner wall thermal oxide film, wherein in step (d), the inner wall thermal oxide film, due to the sidewall formed on the side face of the opening in the protection film, is formed to ***an edge*** of the semiconductor substrate which is ***located at an upper edge portion*** *of the trench*, as recited in claim 70.

The distinction is important because the formation of the inner wall thermal oxide film to an edge of the semiconductor substrate which is located at an upper edge portion of the trench allows an edge of the semiconductor substrate which is exposed at the upper edge portion of the trench to be rounded, thereby preventing field concentration at the edge of the semiconductor substrate in operation of the device. *See e.g.*, Published Application at page 9, paragraph [171]. In contrast, in Sumino, because the sidewall is formed on the upper trench, the side face of the upper trench (40a) cannot be oxidized. As such, Sumino cannot have an effect of allowing an edge of the semiconductor substrate which is exposed at the upper edge portion of the trench to be rounded and preventing field concentration at the edge of the semiconductor substrate.

For at least the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 70.

Claim 77 includes features similar to the above-recited features of claim 70. Therefore, for at least the reasons presented above with respect to claim 70, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 77.

Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Because claims 70 and 77 are allowable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also allowable. In addition, it is respectfully submitted that the dependent claims are allowable based on their own merits by adding novel and non-obvious features to the combination.

For example, claim 90 recites a method for manufacturing a solid-state imaging device, wherein the sidewall is ***not*** formed on the side face of the semiconductor substrate. In contrast and as noted above, in Sumino, the sidewall (50b) is formed on the side face of the semiconductor substrate. For at least this reason and the reasons presented above with respect to claim 70, Applicants respectfully request consideration and allowance of claim 90.

Claim 92 includes features similar to the above-recited features of claim 90. For at least the reasons presented above with respect to claim 90, Applicants respectfully request consideration and allowance of claim 92.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103 be withdrawn.

Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If

there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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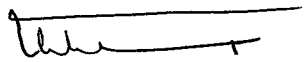

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